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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/089,312	06/02/98	FINDLATER S	CISCP035

TS

WM02/1220
RITTER, VAN PELT, AND YI LLP.
4906 EL CAMINO REAL
SUITE 205
LOS ALTOS CA 94022

EXAMINER	
TON, A	
ART UNIT	**PAPER NUMBER**
2661	8

DATE MAILED: 12/20/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/089,312	Findlater et al.
Examiner	**Group Art Unit**
Anthony Ton	2661

☒ Responsive to communication(s) filed on *Jun 2, 1998*.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-16* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-16* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *4 and 6*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948 (Substitute)

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Object to Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Object to Specification

2. The disclosure is objected to because of the following informalities:

- Page 1 lines 10 and 11, "co-pending U.S. Patent Application No._____" should be listed appropriately, and including filing date.

- Page 4 line 1, it is suggested to change "line 215" to --line 218--

- Page 8 line 4, it is suggested to change "a control data line" to --a transmit control line--

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over RMII™ Consortium (RMII™ Specification, March 20, 1998) in view of Ballance et al. (U.S. Patent 4,748,621).

With respect to claims 1, 15 and 16, a low pin count Reduced Media Independent Interface™ (RMII™) specification is intended for use between Ethernet PHYs and Switch ASICs. The purpose of this interface is to provide a low cost alternative to the IEEE 802.3u [2] MII as specified in Clause 22. Under IEEE 802.3u [2], an MII comprised of 16 pins for data and control is defined. At 6 pins per port and 1 pin per switch ASIC, the proposed RMII™ specification would save 119 pins plus the extra power and ground pins to support those additional pins for a 12 port switch ASIC.

The RMII™ specification has been optimized for use in high port density interconnect devices which require independent treatment of transmit and receive data paths. The RMII™ specification has following characteristics:

1. It is capable of supporting 10Mb/s and 100Mb/s data rates

2. A single clock reference is sourced from the MAC to PHY (or from an external source)

3. It provides independent 2 bit wide (di-bit) transmit and receive data paths

4. It uses TTL signal levels, compatible with common digital CMOS ASIC processes.

In choosing the signaling for the RMII™ specification, the following criteria was applied:

1. Clock frequency of 50MHz or less to minimize EMI (electromagnetic interference) and IC I/O requirements.

2. Pin count independent of port density of the PHY

3. Single synchronous clocking.

4. Reduction of required control pins.

The RMII™ specification differs from the present invention is that the RMII™ provides an MII interface that requires 8 pins (TXD[1:0], TX_EN, RX_ER*, CRS_DV, RXD[1:0], and REF_CLK; note: RX_ER* pin is required output of the PHY, the ASIC may choose to use this input) and run at 50MHz (see Fig. 1, Table 1, and Paras. 1.0 - 5.0), while the present invention provides an MII interface that requires 5 pins (TXD, TXCNTL, RXD, RXCNTL, and CLOCK) using time-division multiplexing and run at 100MHz.

However, the Applicant is using the method and apparatus that were disclosed by the RMII™ specification and applying time-division multiplexing for the functions of 16 pins in the standard MII interface to reduce number of pins for the MII interface between an MAC and an PHY. The RMII™ specification also recites that it is a capable of supporting 10Mb/s and 100Mb/s data rates, and capability for a clock frequency of 100MHz (see lines 8-9 in para. 3.0). In addition, Ballance et al. disclose TDMA/TDM interfacing particularly relating to an interface circuit for interconnecting an TDMA system to an external station, i.e. one which is part of the TDMA system, which station operates a plurality of channels in a time division multiplex format (see col. 1 lines 5-20; and col. 10, lines 1-50).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made would employ such RMII™ Specification by doubling the clock frequency from 50MHz to 100MHz to save 2 more pins on the data paths, and employ the TDM as taught

by Ballance et al. to provide transmit and receive control information that is provided in the standard MII interface (as shown in Figs. 4 and 5 of the present claimed invention).

The motivation/suggestion to do so would have been to employ such pin reduction and time-division multiplexing as suggested by RMII™ specification in Para. 3.0, and by Ballance et al. in col. 10, lines 1-50, respectively.

With respect to claims 2, and 4-6, the RMII™ specification disclose a method of communicating between a MAC and a PHY as recited in claim 1,

wherein the time-division multiplexed receive control signal (see Figs. 2 and 3; and CRS_DV on para. 5.2) includes 4 bit segments and wherein each bit segment includes a synchronization (see Para. 5.2), a receive data valid bit (see the last section in Para. 5.2, and Para. 5.3), a receive error bit (see Para. 5.3.3), and a carrier sense bit (see Para. 5.2).

With respect to claim 3, the RMII™ specification disclose a method of communicating between a MAC and a PHY as recited in claim 2,

wherein the receive data line includes 4 bit segments and wherein the beginning of a 4 bit segment is determined by the synchronization bit (see preamble bits in Fig. 2; and Para 5.3).

Claims 7, and 9-14 are similar to claims 2, and 4-6 for the transmit control signal; therefore, the argument applied above for claims 2, and 4-6 are applicable to claims 7, and 9-14 for their common features.

Claim 8 is similar to claim 3 for the transmit data line; therefore, the argument applied above for claim 3 is applicable to claim 8 for their common features.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. RMII™ Consortium (RMII™ Specification, March 20, 1998) in view of Ballance et al. (U.S. Patent 4,748,621) are cited to show a method and apparatus for reducing pin count Media Independent Interface, which are considered pertinent to the claimed invention.

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Ton whose telephone number is (703) 306-5622. The examiner can normally be reached on Monday through Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Doug Olms,* can be reached on (703) 305-4703. The fax phone for this group is (703) 305-3988. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Anthony Ton
December 8, 2000

DANG TON
PRIMARY EXAMINER